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| OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. | | | EXAMINER | | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

4m Application N . Applicant(s) 09/891,129 NISHIYAMA ET AL. Office Action Summary Examiner Art Unit Anh D. Mai 2814 -- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). **Status** Responsive to communication(s) filed on 06 June 2003. 1)🛛 This action is FINAL. 2b) This action is non-final. 2a)□ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disp sition of Claims 4) \boxtimes Claim(s) <u>1-4,6-9 and 12-26</u> is/are pending in the application. 4a) Of the above claim(s) 14 and 15 is/are withdrawn from consideration. 5) Claim(s) _____ is/are allowed. 6) Claim(s) 1-4,6-9,12,13 and 16-26 is/are rejected. 7) Claim(s) _____ is/are objected to. 8) Claim(s) _____ are subject to restriction and/or election requirement. **Application Papers** 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on ____ is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). 11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner. If approved, corrected drawings are required in reply to this Office action. 12) The oath or declaration is objected to by the Examiner. **Priority under 35 U.S.C. §§ 119 and 120** 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) \square All b) \square Some * c) \square None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)

a) The translation of the foreign language provisional application has been received. 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

4) Interview Summary (PTO-413) Paper No(s).

Notice of Informal Patent Application (PTO-152)

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submissions filed on March 25, 2003 and June 6, 2003 have been entered.

Status of the Claims

2. Amendments filed March 25, 2003 and June 6, 2003 have been entered as Paper No. 15 and 19, respectively. Claims 1, 4, 16 and 17 have been amended. Claims 1-4, 6-9 and 12-26 are pending. Claims 14 and 15 have been withdrawn.

Specification

- 3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
- 4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: SEMICONDUCTOR DEVICE HAVING A HIGH-K METAL OXIDE AND SILICON OXIDE COMPOUND INSULATING FILM .

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Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2 and 19 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 2 and 19 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in Paper No. 19 filed June 6, 2003. In that paper, applicant has stated "In the claimed invention, to obtain nano-crystals having a particle diameter within a range of between 1 nm and 10 nm the insulating film is an oxide. The applicants note that if nitrogen in contained in the insulating film, crystallization is inhibited and the insulating film becomes amorphous. As a result, applicants note that if nitrogen is contained in the insulating film nano-crystals having a particle diameter within a range of between a nm and 10 nm cannot be obtained." (See page 4, 3rd paragraph), and this statement indicates that the invention is different from what is defined in the claim(s) because the insulating materials of claims 2 and 19 clearly comprise nitrogen (nitride or oxynitride), which inhibits crystallization.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-4, 7-9, 12, 13, 16-19 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anthony et al., (J.P Patent No. 11-135774) in view of Applicant Attachment (Paper No. 19, filed June 6, 2003) or M.R. Visokay et al. of record (IDS Paper No. 8).

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With respect to claim 1, Anthony teaches a semiconductor device substantially as claimed including:

a semiconductor substrate (20); and

a circuit element using an insulating film (36) formed in the semiconductor substrate (20), the insulating film (36) containing a silicon compound containing oxygen, and a metal compound containing a metal other than silicon and oxygen, the insulating film (36) further comprising crystals. (See Fig. 8, page 27, line 14-page 28, line 14).

With respect to the size of the nano-crystals, although Anthony does not explicitly disclosing the particle diameter of the crystals.

However, Anthony clearly teaches that the silicate 36 is subjected to a high temperature anneal to densify or *crystallize* (page 28, lines 5-7). Additionally, Applicant Attachment (Fig. (a)) and Visokay (Fig. 3b) disclose the diameter of the crystals of the insulating film to be within the claimed range (1nm – 10nm).

With respect to claim 16, Anthony teaches a semiconductor device substantially as claimed including:

a semiconductor substrate (20);

source and drain regions (140/160) formed apart from each other in the semiconductor substrate;

a gate the insulating film (36) formed between the source and drain regions (140/160), the gate insulating film (36) containing a silicon compound containing oxygen, and a metal

compound containing a metal other than silicon and oxygen, the insulating film (36) further comprising crystals; and

a gate electrode (38) formed on the gate insulating film (36). (See Figs. 1 and 9, page 27, line 14-page 28, line 14).

With respect to the size of the nano-crystals, the similar reason as that of claim 1 is also applied here.

With respect to the source and drain regions, although does not explicitly disclosing in the invention, however, the gate insulating layer (36) of Anthony is intended as the substitute for the regular silicon oxide layer (180), thus, the structure of the MOSFET (Fig. 1) is unchanged.

With respect to claims 2 and 17, as best understood by the examiner, the silicon compound of Anthony is a compound selected from the group consisting of a silicon oxide.

With respect to claims 3 and 18, the crystal of Anthony are made of the metal compound.

With respect to claims 4 and 19, as best understood by the examiner, the nano-crystal of Anthony is made of an oxide.

With respect to claims 7 and 21, the semiconductor device of Anthony further includes a silicon oxynitride film formed between the semiconductor substrate and the insulating film. (See page 21, 1l. 23-25).

With respect to claims 8 and 22, the metal other than silicon of Anthony is at least one of metal selected from the group consisting of La, Y, Ta, Zr, Hf. (See page 23, ll. 12-24).

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With respect to claim 9, the circuit element of Anthony is a MOSFET and the insulating film (36) is a gate insulating film of the MOSFET.

With respect to claims 12 and 23, Anthony teaches: near the silicon interface the silicate has a large SiO₂ component, while the upper portion of the silicate layer has a large metal oxide component. (page 16, lines 10-12). Anthony further adds: assumes that a protective or native silicon oxide region 26 (preferably comprising less than 1nm of oxide).

Note that the specification contains <u>no disclosure</u> of either the critical nature of the claimed: distance of 0.7nm from the interface of any unexpected results arising therefrom.

Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. In re

Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, at least one of the nano-crystals of Anthony is position away from the interface of the silicon substrate and the insulating film by a distance of *less than 1nm*, which approximate the claimed range.

With respect to claims 13 and 24, the insulating film (36) of Anthony is a mixed film containing silicon compound and metal compound.

With respect to claim 25, the gate electrode (38) of Anthony includes polycrystalline silicon layer.

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7. Claims 6 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anthony '774, Applicant Attachment and Visokay et al., as applied to claims 1 and 16 above, and further in view of Wilk (U.S. Patent No. 6,544,875).

Anthony teaches the dielectric layer may be made substantially thicker than a conventional gate dielectric with equivalent field effect. (See Summary pages 15-16).

Thus, Anthony is shown to teach all the features of the claim with the exception of explicitly disclosing the thickness of the insulating layer (36).

However, Wilk teaches a high dielectric constant and low leakage dielectric material is formed to a thickness (4nm-10nm) that overlaps the claimed range (3nm-20nm). (col. 3, lines 40-57).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the insulating film (36) of Anthony to the thickness as taught by Wilk to form a high dielectric constant layer for the miniature MOSFET device.

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anthony '774, Applicant Attachment and Visokay et al., as applied to claim 16 above, and further in view of Bai et al. (U.S. Patent No. 5,818,092) of record.

Anthony teaches all the features of the claim with the exception of further includes silicide layers formed on the source and drain regions (140/160).

However, Bai teaches field effect transistor (100) formed on a semiconductor substrate (101) further includes silicide layer (114) formed on the source and drain regions (110).

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Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further includes silicide layers on the source and drain regions (140/160) of Wallace as taught by Bai to reduce sheet resistance. (See col. 1, lines 13-22).

Response to Arguments

9. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M

August 8, 2003